



Data Sheet

*JV9000*  
**Adjustable Vcc  
Noise Generator**



**Count on the noise leader**

## Noisecom JV9000

Today's computers, communication devices and other electronic equipment use a combination of digital ICs (both LSI and VLSI), analogue ICs, and A/D and D/A converters. Due to space constraints, these components are packed within a very small space, which again provides ideal conditions for electromagnetic interference (EMI). Circuit designers are well aware of noise and jitter effects on clock and data lines; effects that may threaten data integrity and proper functionality of their systems. They take great care suppressing such disturbance sources. Once causes of such unwanted noise are pinpointed, their effects can be minimized which again, guarantees optimal operation with minimal BER problems.

A "new" kind of noise starts to interfere with the functionality of electronic systems: Vcc and Ground noise, with major culprits called GND Bounce and Vcc Droop Jitter. While Vcc specifications of integrated circuits define the operational range, high frequency noise can disturb their functionality. This, even operating within specified Vcc limits. Such disturbances can enter the circuits through residual capacities on the chip. Designers and manufacturers of integrated circuits need to ensure their products offer sufficient margin against Vcc noise, making them tolerant against noise at these paths. The usual recommendation of placing a blocking capacitor adjacent to the VCC pin may no longer be sufficient.



Noisecom JV9000

Noisecom's JV9000 is a generator specifically designed to inject noise and deterministic jitter (DJ) signals into Vcc lines (see figure 1). The system is very easy to set up and requires in its basic setup only two connections: Vcc power to the Vcc input of the JV9000, and its output connected to the Vcc path of the DUT test board. The built-in noise generator offers an output noise power of 0dBm nominal and can be reduced in 1dB steps with a 100dB attenuator.

The JV9000 has an optional CW generator that delivers various frequencies with an output power of 0dBm that can be attenuated. This provides a source simulating signals that are usually generated by the switching frequencies of power supplies. Noisecom's JV9000 generator can be optionally equipped with one or more auxiliary inputs that allow adding external signals onto the Vcc line.

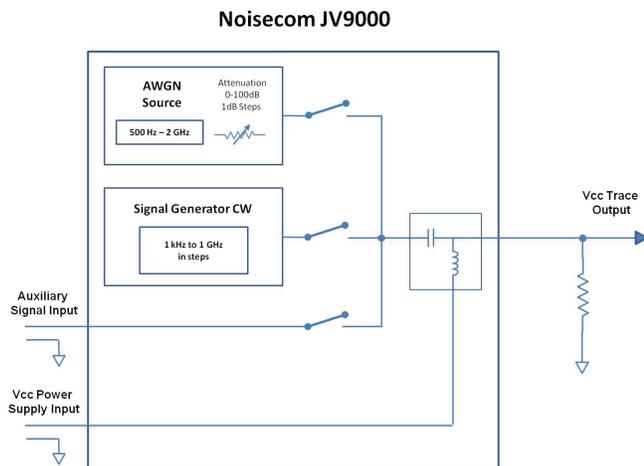


Figure 1. Noisecom Vcc Noise and CW Generator

Impedances of both, the noise source and signal generator is 50 Ohms. The impedance of the Bias-T is a function of frequency and therefore variable. Impedance of DUTs varies widely because many factors play a role, including operational frequency and switching speeds. Frequency dependent behavior does not allow for matching impedance between the generator and DUT, but with 0dBm output power, the generator is powerful enough to add the required noise energy to the Vcc path allowing testing tolerance limits of most DUTs.

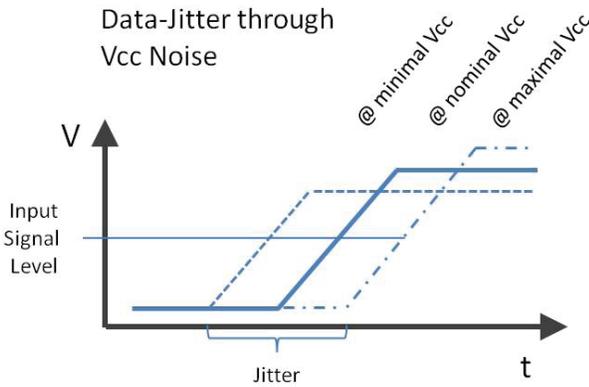


Figure 2. Data jitter can be caused through Vcc and GND noise

### Why Does Vcc Noise Influence System Functionality?

Switching behavior of digital circuits depends on defined threshold levels, that determine if a signal is considered a logical "1" or "0". Figure 2 shows that switching time can shift with varying Vcc levels, even if data input signal levels are constant. While chip designers try to minimize jitter effects caused by Vcc variations, their effects cannot completely be eliminated. Digital threshold decisions are to some degree always depending on the Vcc power level, even if Vcc varies just within its allowed limits. While general chip functionality is provided within that Vcc range and the IC works as specified, Vcc variations cause slight changes in the switching responses. This means: Vcc and GND noise cause output signal jitter.

Analog circuits respond to noise present in Vcc or GND lines. The effects can even multiply if the circuit amplifies signals. Whether a high speed digital IC, a precision linear device or a combination of both, like a PLL requiring precision threshold levels are used, Vcc noise will usually influence timing and purity of output signals. Vcc noise generated directly on the chip can even create unwanted noise loops, which again can significantly influence functionality of electronic systems. Testing against Vcc noise helps designers to guaranty flawless functionality of their circuits.

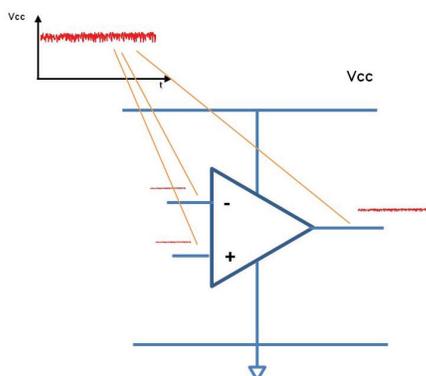


Figure 3.

### Causes of VCC Noise

Close proximity of high-speed data traces in PCB layouts can create distortions caused by Inter Symbol Interference (ISI), Inter Carrier Interference (ICI) or other unwanted distortion. Power supplies are well known for generating deterministic jitter (DJ), effecting both, power traces and data lines. The cause can be linked to power supply switching frequencies and their harmonics. Every electronic component, passive or active, generates a distinct amount of noise energy, caused by thermal random movement of charge carriers and amplifying (active) devices multiply this and any other noise. These problems are a well known and particular care should be taken on data and clock lines. Circuit designers are facing a new problem with both analog and digital domains: increasing switching speed of integrated circuits, devices can cause noise problems at VCC or Ground lines.

Both, GND planes and Vcc lines have usually extremely low impedance. This fact has rendered noise so far negligible. Use of block capacitors in close proximity to the chips' power and GND pins helped reducing any jitter and bounce effects. Unfortunately, these measures cannot eliminate effects completely, particularly not if the noise is generated within circuit. In a very fast switching environment, inherent line inductances and capacitances cause frequency dependent jitter on data lines and they generate noise at GND and Vcc lines. This effect is called Vcc-Droop Jitter and Ground Bounce. The faster circuits switch, the more noise they generate. The effects are multiplied with simultaneously switching (parallel) I/O ports.

As described above digital circuits process data either as logical "1" or as logical "0". Figures 4 and 5 show simplified digital I/O ports. Image 4 depicts the active parts switching, from "0" to "1", image 5 shows an output change from "1" to "0".

Thresholds determining the logical state are directly dependent from the level potential difference between GND and Vcc. Noise from either plane can cause early or delayed output response. In extreme cases, it will result in spikes at the output ports, and cause unrecognized information on the data bus. Clean and stable Vcc and Ground levels are mandatory to prevent such disturbances that can significantly influence system functionality.

### Self induced Vcc and GND Noise

Ground Bounce occurs when integrated circuits switch their high-speed output ports from "1" to "0"; Vcc Droop happens when they switch from "0" to "1". With Ground Bounce, the device ground rises relative to the power supply ground. Conversely, with Vcc Droop Jitter, device Vcc drops relative to the power supply Vcc. The amount of bounce or droop depends on the rise or fall times of the switching output ports. It multiplies with the number of simultaneously switched output pins.

### Ground Bounce

Figure 4 illustrates the path between power supply, board, device output and output trace. The path can be described as four inductances, ( $L1_{GND}$  to  $L4_{GND}$ ) that are connected in line, supplying the die GND. Voltage response of inductances is a function of current and change time, resulting voltage can be described as in the following equation:  $V = L_{sum} \times (di / dt)$

V is the voltage difference between the die Vcc and power supply Vcc,  $L_{sum}$  is the sum of all path inductances ( $L1, L2, L3$  and  $L4$ ), and  $di$  the time increment in which the current change happens.

An inherent capacity within all data output traces plays also an important role. This capacitance is charged as the output drives a logical "1". When the output switches back to "0", the charge has to be released through the Lo-transistor, resulting in a current initiated from the data trace capacitance to the die pin ground and it continues to the power supply ground. Because of relatively small data path capacities, these currents are quite small but because of the in-line inductances, it can cause significant spikes with fast switching times. Block capacitors adjacent to the chip pins cannot eliminate all of the energy from these spikes.

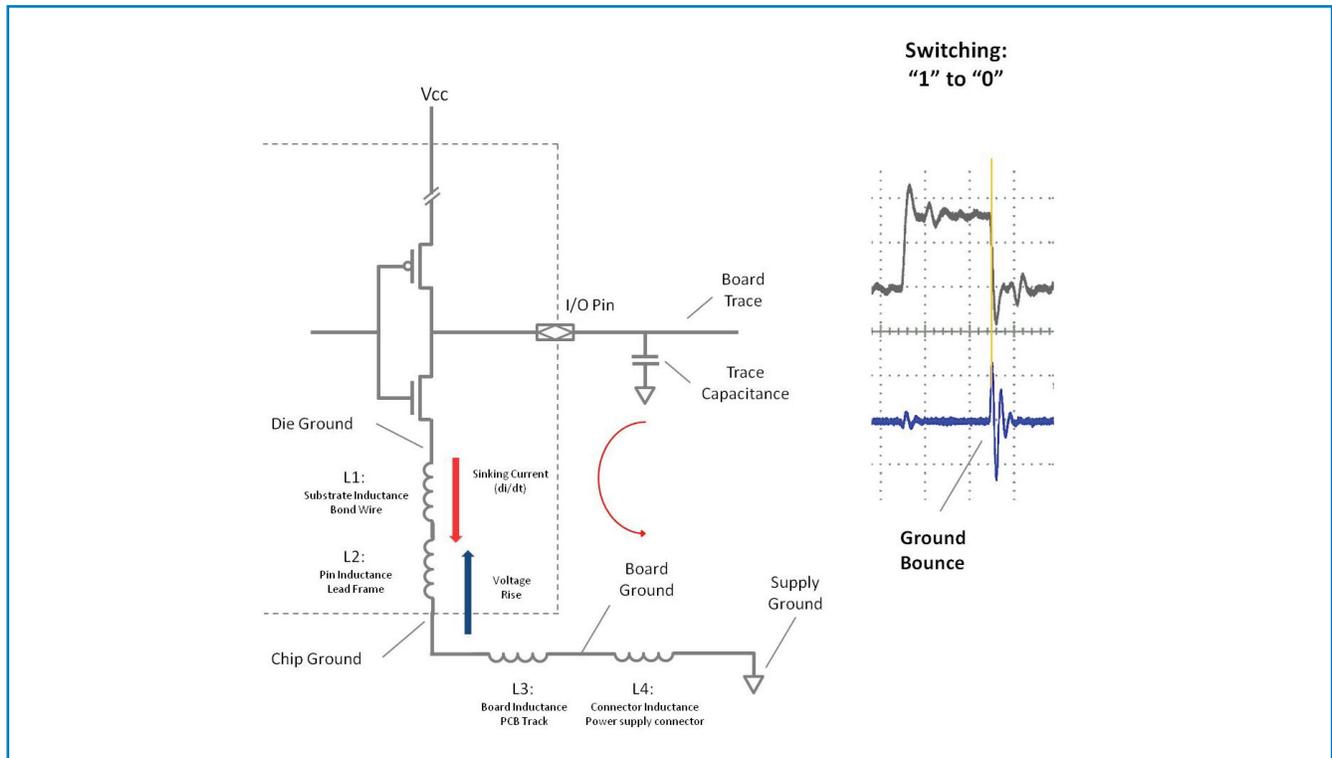


Figure 4.

### Vcc-Droop Jitter

Conversely, VCC droop Jitter occurs when ICs switch outputs from "0" to "1" at high speed. Die Vcc drops relative to the Power Supply Vcc. Figure 5 shows the connections between power supply, board, device, and the output trace capacitance; all connected via the Hi-transistor. Because trace capacitance discharge current has to pass inductances  $L1_{Vcc}$  to  $L4_{Vcc}$ , any current change produces a voltage difference between the device die Vcc and power supply Vcc. The amount of voltage is, as with GND bounce, specified with the equation above, and  $L_{sum}$  is the sum of all inductances in the Vcc path.

### Conclusion

Unwanted noise is introduced in all electronic circuits, and all switching devices induce GND and Vcc noise. Additional sources add their part of noise onto clock lines, data busses, reference lines and more. Finally, power supply ripple and noise caused by load changes effects as well. Providing sufficient noise margin for Vcc and GND specifications is paramount for flawless functionality of integrated circuits. This document shows that it is of great importance measuring device responses to external and internal noise generation. Noisecom's JV9000 is developed to provide developers a tool that allows them to measure their circuits easily. It should not be missing in any developers' lab.

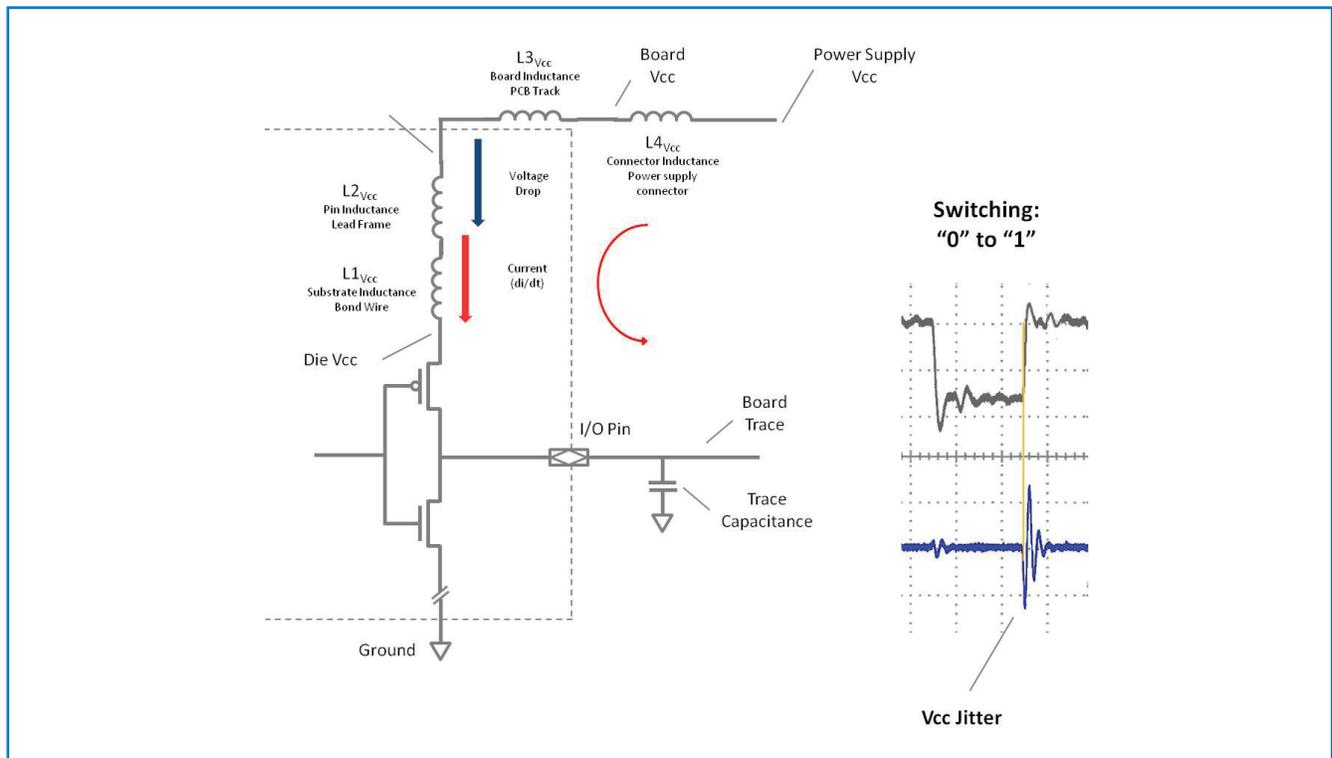


Figure 5.

## Specifications

### Input

Maximum Voltage	5V
Maximum Current	250mA (other on request)
Connector	SMA

### Output

Maximum Voltage	same as input
Maximum Current	same as input
Connector	same as input

### Noise Source (white Gaussian noise)

Impedance	50 Ohms
Frequency Range	500 Hz to 2 GHz
Output Power (after Bias-T)	0dBm

### Frequency Generator

Impedance	50 Ohms (typ.)
Frequency Range	1 kHz, 3 kHz, 10 kHz, 30 kHz, 100 kHz, 300 kHz, 1MHz, 3 MHz, 10 MHz, 30 MHz, 100 MHz, 300 MHz, 1 GHz
Output power (after bias-T)	0 dBm

### Auxiliary Input

Maximum voltage	same as input
Maximum current	same as input
Connector	same as input
Frequency Range	1 kHz to 1 GHz

### General Specifications

Dimensions (W/H/D)	17in x 5.25in x 13in / 432mm x 133mm x 330mm
Line Power	120V, 60Hz 1.5A
Operating Temperature	-10°C to 60°C / 14°F to 140°F

### Options

N6/N8opt03	230V, 50Hz
NC6/NC8opt7	N female output connectors
NC6/NC8opt8	BNC female output connectors

Please contact factory for other options or modifications

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